Freeform Search

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term: `L18 and 13 and 14 and 15 and 16 and 17 and (18 with 19) and 111 and 112`

Display: `50` Documents in **Display Format:** `-` **Starting with Number** `1`

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

| Search | Clear | Interrupt |

Search History

DATE: Thursday, February 19, 2004   Printable Copy   Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L19	L18 and 13 and 14 and 15 and 16 and 17 and (18 with 19) and 111 and 112	18	L19
L18	11 near3 113	5320	L18
L17	114 and 12 and 13 and 14 and 15 and 16 and 17 and 18 and 19 and 110 and 111 and 112	11	L17
L16	114 and 12 and 13 and 14 and 15 and 16 and 17 and 18 and 19 and 110 and 111 and 112	11	L16
L15	L14 same 13 same 14 same 15 same 17	0	L15
L14	11 adj5 L13	4083	L14
L13	adc$1 or (analog adj3 digital)	228128	L13
L12	bias$3	954337	L12
L11	gain$1	471099	L11
L10	current	2558731	L10
L9	shift$3	1338869	L9
L8	level$	2936820	L8
L7	transistor$1	683931	L7

h   e b   b g e e e   e c   f ff e ch

L6	amplification or amplif$	959901	L6
L5	latch$3	513606	L5
L4	bipolar	118193	L4
L3	reset$	459181	L3
L2	cmos	100977	L2
L1	compar$	2799355	L1

END OF SEARCH HISTORY

h   e b   b g e e e   e c   f ff e ch

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Term:
L11 and l10

Display: 50 Documents in **Display Format:** - **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search | Clear | Interrupt

Search History

DATE: **Thursday, February 19, 2004** <u>Printable Copy</u> <u>Create Case</u>

<u>Set Name</u> side by side	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L13</u>	L11 and l10	6	<u>L13</u>
<u>L12</u>	L11 and l10	6	<u>L12</u>
<u>L11</u>	341/$.ccls.	35522	<u>L11</u>
<u>L10</u>	L9 and cmos	33	<u>L10</u>
<u>L9</u>	L8 and current	114	<u>L9</u>
<u>L8</u>	L7 and (adc$1 or (analog adj3 digital))	116	<u>L8</u>
<u>L7</u>	compar$ and (level with shift$3 with transistor$1) and latch$3 and (amplification or amplif$) and reset$ and (switch$3 or select$3) and bias$3	371	<u>L7</u>
<u>L6</u>	L2 and (adc$1 or (analog adj3 digital))	9	<u>L6</u>
<u>L5</u>	L2 and (adc$1 or (analog adj3 digital))	9	<u>L5</u>
<u>L4</u>	L2 and (adc$1 or (analog adj3 digital))	9	<u>L4</u>
<u>L3</u>	L2 and (adc$1 or (digital adj3 analog))	17	<u>L3</u>
<u>L2</u>	L1 and compar$	123	<u>L2</u>
<u>L1</u>	(level adj shift) adj transistor$1	243	<u>L1</u>

h   e b   b g e e e   g   f ff e ch